CLAIMS:

1. Modulator for generating a digital I/Q signal having a plurality of time-slots, the modulator comprising means for introducing a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots of the plurality of time-slots.

2. Modulator according to claim 1, wherein the means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots of the plurality of time-slots comprises a digital multiplier for multiplying the I signal and the Q signal of the I/Q signal with a dip-shaped waveform.

3. Modulator according to claim 1, further comprising a pulse shaping filter and wherein the means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots comprises means for generating a step-off response followed by a step-on response of the pulse shaping filter such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots.

4. Modulator according to claim 3, wherein the means for generating the step-off response followed by the step-on response of the pulse shaping filter comprises means for filling digital zeros into the pulse shaping filter during the guard interval such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots.

5. Modulator according to claim 3, further comprising a GMSK modulator

with a linear branch and a quadratic branch and a multiplexer, wherein the multiplexer feeds complex zeros into the branches such that the step-off response is followed by a step-on response of the pulse shaping filter such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots.

6. Modulator in accordance with claim 1, wherein the modulator is a GMSK modulator and a 8PSK modulator.

7. Signal processing method for generating a digital I/Q signal having a plurality of time-slots, the signal processing method comprising the steps of:

(a) modulating the I signal and the Q signal for generating the I/Q signal; and

(b) introducing a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots of the plurality of time-slots.

8. Signal processing method according to claim 7, further comprising the step of multiplying the I signal and the Q signal of the I/Q signal with a dip-shaped waveform.

9. Signal processing method according to claim 7, wherein step (b) of introducing the dip in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots further comprises the step of:

generating a step-off response followed by a step-on response of the pulse shaping filter such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots.

10. Computer program for generating a digital I/Q signal having a plurality of time-slots, in particular for a chipset for implementing a TDMA transmitter in a

GSM-, EDGE- or EGPRS-system, the computer program comprising the steps of:

(a) modulating the I signal and the Q signal for generating the I/Q signal; and

(b) introducing a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots of the plurality of time-slots.

11. Transmitter comprising a modulator according to claim 1.